REMARKS

In view of the above amendments and following remarks, further examination is respectfully requested.

The specification and abstract have been reviewed and revised to improve their English grammar and U.S. form. The amendments to the specification and abstract have been incorporated into a substitute specification and abstract. Attached are two versions of the specification, a marked-up version showing the revisions, as well as a clean version. No new matter has been added.

The Examiner objected to the specification based on the informalities listed on pages 3-4 of the Office Action. These informalities have each been addressed in the above-mentioned amendments to the specification. However, regarding the objection to page 17, line 12 of the specification, it is respectfully submitted that the phrase "a branch are issued," when taken in the full context of the entire sentence, is correct. That is, the sentence recites "and the instructions that are not executed because of a branch are issued simultaneously." When taken in the context of the entire sentence, the verb "are" refers back to the subject "instructions." Thus, when taken in the full context of the sentence there is proper subject-verb agreement and there are no grammatical inconsistencies.

Claim 7 was objected to under 37 CFR § 1.75(d)(1) based on the phrase "an acception unit." However, it is noted that the word "acception" is a recognized word in the English language (see attached Dictionary.com print-out citing Webster's Revised Unabridged Dictionary, 1996, acception: "a receiving, accepting"). Therefore, it is submitted that the phrase "an acception unit" is grammatically correct. Please note that the phrase "an acceptation unit" within the specification has been changed to "an acception unit" so that the specification is consistent with claim 7.

Claim 21 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner rejected claim 21 based on insufficient antecedent basis for the element "the reconstruction apparatus." This rejection is clearly inapplicable to amended claim 21 because claim 21 has been corrected to recite "said reconstruction unit."

Claims 1-9, 22, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto et al. (US Patent Publication 2003/0204819) in view of Moller et al. (US Patent 6,826,522). Claims 10-13 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto in view of Moller, and further in view of Ussery et al. (US Patent Publication 2001/0025363). Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto in view of Moller, and further in view of Ussery and Miyake et al. (US Patent 6,681,280). These rejections are respectfully traversed, and it is submitted that these rejections are clearly inapplicable to amended claims 1-23, for the following reasons.

The present invention is a simulation apparatus having two simulation units, wherein each simulation unit simulates the execution of the same group of instructions intended to be simultaneously executed. The first simulation unit simulates a simultaneous execution of the instructions intended to be simultaneously executed. The second simulation unit simulates a sequential execution of the same group of instructions based on the result of the simultaneous execution of those instructions. These distinguishing features of the present invention are discussed below in relation to the prior art of record.

Amended Claims 1-21 are Patentable Over Matsumoto in View of Moller

Amended independent claim 1 recites a simulation apparatus for simulating a very long instruction word (VLIW) processor, the simulation apparatus including, (1) a first simulation unit operable to simulate execution of a group of instructions intended to be simultaneously executed (i.e., *simultaneous execution*), and operable to generate a first simulation result; and (2) a second simulation unit operable to simulate, based on the first simulation result generated by the first simulation unit, a sequential execution of the same group of instructions on an instruction-by-instruction basis (i.e., *sequential execution*), and to generate a second simulation result.

In contrast to the present invention as recited in amended claim 1, Matsumoto teaches a method of generating a development environment which includes the generation of a simulator (see paragraph 0011, lines 1-6 and 13-14). The simulator is capable of simulating a VLIW processor and simulating an execution of an application on

the simulated VLIW processor for the purpose of understanding the performance of a processor in a short time (see paragraph 0387, lines 3-6; paragraph 0011, lines 1-6 and 13-14; and paragraph 0010).

Initially, the Examiner acknowledges that the Matsumoto reference does not teach the simultaneous execution of a group of instructions intended to be simultaneously executed (see Office Action page 6, paragraph 3), as required by claim 1. Rather, based on the discussion above, it is clear that Matsumoto teaches a simulation which merely includes a single simulator for simulating an application on a simulated processor for understanding a processor's performance in a short period of time. Thus, as acknowledged by the Examiner, Matsumoto does not disclose or suggest the simulation of simultaneous execution of a group of instructions intended to be simultaneously executed.

In addition, although Matsumoto teaches the simulation of a VLIW processor, the simulation of Matsumoto is not a simulation of sequential execution of instructions based on the result of the simultaneous execution of those same instructions intended to be simultaneously executed, as required in independent claim 1.

Accordingly, it is respectfully submitted that the Matsumoto reference does not disclose or suggest a simulation of the simultaneous execution of a group of instructions intended to be simultaneously executed, and also does not disclose or suggest a simulation of sequential execution of instructions based on the result of the simulation of the simultaneous execution of those same instructions. Thus, Matsumoto does not disclose or suggest the simulation of the first simulation unit or the simulation of the second simulation unit, or any combination thereof, as required in independent claim 1.

The Examiner cited the Moller patent for teaching a second simulation unit operable to generate a simulation result of the group of instructions on an instruction-by-instruction basis based on a simulation result generated by the first simulation unit (see Office Action page 7, paragraph 1). It is noted that Moller teaches that each instruction includes multiple processing stages, wherein each processing stage of each instruction includes a fetch, decode, execute, and condition return operation (see Fig. 3). Further, Moller teaches a simulation of a VLIW processor by reordering the timing of the execution of multiple processing stages of instructions (see col. 2, lines 13-31; col.

8, lines 27-34). Accordingly, Moller teaches that within a single cycle of the simulation of the VLIW processor the fetch, decode, execute, and condition return operations are simultaneously executed, wherein the fetch, decode, execute, and condition return operations are processing stages of various instructions based on the reordering taught by Moller (see Fig. 3, cycle 3, 4, and 5; referring to cycle 5, the stages which are simultaneously executed are from instruction 5, 4, 3, and 2). This reordering of processing stages results in only one simulation of each processing stage of an instruction (see Abstract, Fig. 3, and 4). Thus, any simultaneous execution taught by Moller refers to the simultaneous execution of a set of processing stages (i.e., fetch, decode, execute, and condition return) that do not come from the same instruction, but rather come from multiple instructions which were not intended to be simultaneously executed.

To better illustrate the differences between the simultaneous execution of a group of instructions intended to be simultaneously executed, as required by claim 1, and the simultaneous execution of reordered processing stages, as disclosed by Moller, please refer to the figure shown in attached Example 1. This figure shows (1) a circled group of instructions intended to be simultaneously executed, as required by claim 1, and (2) a circled set of reordered processing stages of instructions, as disclosed by Moller.

Specifically, Example 1 illustrates that instructions Ax, Ay, and Az each contain stages IF (i.e., fetch stage), DC (i.e., decode stage), EX (i.e., execute stage), and WB (i.e., write back stage). As illustrated, an exemplary group of instructions intended to be simultaneously executed includes (1) the execution stage EXx from instruction Ax, (2) the execution stage EXy from instruction Ay, and (3) the execution stage EXz from instruction Az. Accordingly, the group of instructions intended to be simultaneously executed requires that the same stage (i.e., execution stage) from each instruction Ax, Ay, and Az be simultaneously executed (see attached Example 1; Fig. 5 of present application). Other exemplary groups of instructions intended to be simultaneously executed, as shown in Example 1, include (1) fetch stages IFx, IFy, and IFz, from instructions Ax, Ay, and Az, respectively, (2) decode stages DCx, DCy, and DCz from instructions Ax, Ay, and Az, respectively, and (3) write back stages WBx, WBy, and WBz from instructions Ax, Ay, and Az, respectively.

On the other hand, referring to Example 1, the simultaneous execution of reordered processing stages taught by Moller refers to the simultaneous execution of a set of processing stages (i.e., fetch, decode, execute, and condition return). The circled set of exemplary reordered processing stages of instructions simultaneously executed includes the simultaneous execution of (1) the EX stage of instruction Ax, (2) the DC stage of instruction Bx, and (3) the IF stage of instruction Cx.

Based on the discussion above, it is clear that Moller discloses a single execution of a set of processing stages (i.e., execution stage, decode stage, and fetch stage) of an instruction, not intended to be simultaneously executed, by reordering the timing of the multiple processing stages. However, Moller does not disclose or suggest a simultaneous execution of instructions intended to be simultaneously executed (i.e., execute stage EXx, EXy, and EXz from instructions Ax, Ay, and Az, respectively), and does not disclose or suggest a sequential execution of the same group of instructions based on the result of the simultaneous execution, or any combination thereof. Specifically, Moller teaches the simultaneous single execution of stages of instructions not intended to be simultaneously executed, but does not disclose or suggest two executions of the same group of instructions, as required by claim 1.

Thus, it is apparent that neither of the Matsumoto and Moller references, whether viewed individually or in combination, discloses or suggests the use of the simultaneous execution of instructions, **and** the sequential execution of the same instructions based on the result of the simulation of the simultaneous execution of those instructions.

Accordingly, the combination of Matsumoto in view of Moller fails to disclose or suggest the features of independent claim 1. It is therefore submitted that a person having ordinary skill in the art would not have been motivated to modify the Matsumoto patent in view of the Moller patent in such a manner as to result in or otherwise render obvious the present invention of claim 1. Thus, it is submitted that claims 1-21 are patentable over Matsumoto in view of Moller.

Amended Claims 22-23 are Patentable Over Matsumoto in View of Moller

Amended claims 22-23 recite a method for simulating a VLIW processor, the simulation method includes generating a first simulation result, and generating a second simulation result. This generation of the first and second simulation result is achieved in the same manner as the generation of the first and second simulation results recited in amended claim 1. Thus, for the same reasons discussed above, it is respectfully submitted that the combination of Matsumoto in view of Moller fails to disclose or suggest the features of claims 22-23. Thus, it is submitted that claims 22-23 are patentable over Matsumoto in view of Moller.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance and an early notification thereof is earnestly requested. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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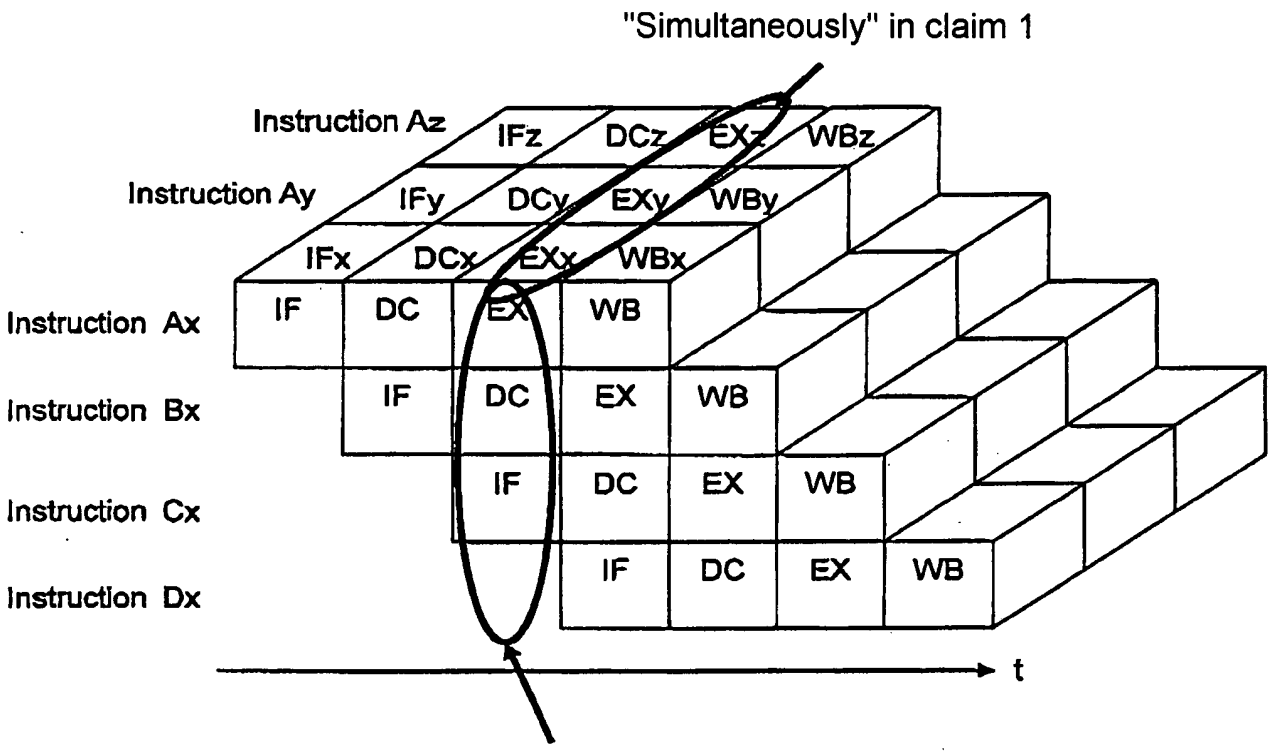
Example 1



IF: Instruction Fetch Stage
DC: Instruction Decode Stage
EX: Instruction Execution Stage
WB: Write Back Stage

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Webster's Revised Unabridged Dictionary - *Cite This Source*
Acception

\Ac*cep"tion\, n. [L. acceptio a receiving, accepting: cf. F. acception.] Acceptation; the received meaning. [Obs.]

Here the word ``baron'' is not to be taken in that restrictive sense to which the modern acception hath confined it. --Fuller.

Acception of persons or faces (Eccl.), favoritism; partiality. [Obs.] --Wyclif.

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